

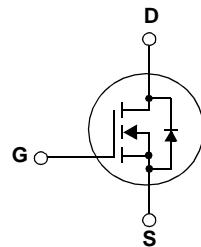
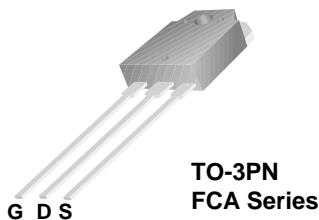
FCA16N60N

N-Channel MOSFET

600V, 16A, 0.170Ω

Features

- $R_{DS(on)} = 0.17\Omega$ (Typ.) @ $V_{GS} = 10V$, $I_D = 8A$
- Ultra low gate charge (Typ. $Q_g = 40.2nC$)
- Low effective output capacitance
- 100% avalanche tested
- RoHS compliant



Description

The SupreMOS MOSFET, Fairchild's next generation of high voltage super-junction MOSFETs, employs a deep trench filling process that differentiates it from preceding multi-epi based technologies. By utilizing this advanced technology and precise process control, SupreMOS provides world class Rsp, superior switching performance and ruggedness.

This SupreMOS MOSFET fits the industry's AC-DC SMPS requirements for PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.

MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted*

Symbol	Parameter		FCA16N60N	Units
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage		± 30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ C$)	16.0	A
		-Continuous ($T_C = 100^\circ C$)	10.1	
I_{DM}	Drain Current	- Pulsed	(Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	mJ
I_{AR}	Avalanche Current		5.3	A
E_{AR}	Repetitive Avalanche Energy		1.34	mJ
dv/dt	MOSFET dv/dt Ruggedness		100	V/ns
	Peak Diode Recovery dv/dt		(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ C$)	134.4	W
		- Derate above $25^\circ C$	1.08	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	$^\circ C$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FCA16N60N	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.93	
$R_{\theta CS}$	Thermal Resistance, Case to Heat Sink (Typical)	0.24	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCA16N60N	FCA16N60N	TO-3PN	-	-	30

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{mA}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	600	-	-	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{mA}$, Referenced to 25°C	-	0.73	-	$^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{V}, V_{GS} = 0\text{V}$	-	-	10	μA
		$V_{DS} = 480\text{V}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 8\text{A}$	-	0.170	0.199	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}, I_D = 8\text{A}$	-	20	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1630	2170	pF
C_{oss}	Output Capacitance		-	70	95	pF
C_{rss}	Reverse Transfer Capacitance		-	5	10	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	40	60	pF
$C_{oss\text{eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{V} \text{ to } 480\text{V}, V_{GS} = 0\text{V}$	-	176	-	pF
$Q_{g(\text{tot})}$	Total Gate Charge at 10V	$V_{DS} = 380\text{V}, I_D = 8\text{A}$ $V_{GS} = 10\text{V}$	-	40.2	52.3	nC
Q_{gs}	Gate to Source Gate Charge		-	6.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	12.9	-
ESR	Equivalent Series Resistance (G-S)	Drain Open		2.9		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{V}, I_D = 8\text{A}$ $R_G = 4.7\Omega$	-	15.8	41.6	ns
t_r	Turn-On Rise Time		-	15.5	41.0	ns
$t_{d(off)}$	Turn-Off Delay Time		-	60.3	130.6	ns
t_f	Turn-Off Fall Time		(Note 4)	-	20.2	50.4

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	16	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	48	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 8\text{A}$	-	1.2	V	
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 8\text{A}$	-	319	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt = 100\text{A}/\mu\text{s}$	-	4.4	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 5.3\text{A}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 16\text{A}$, $dI/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 380\text{V}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

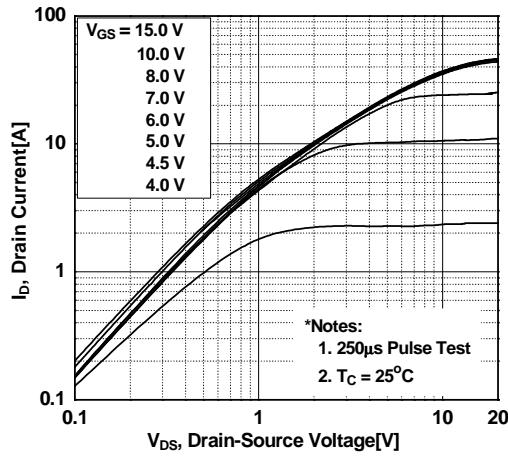


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

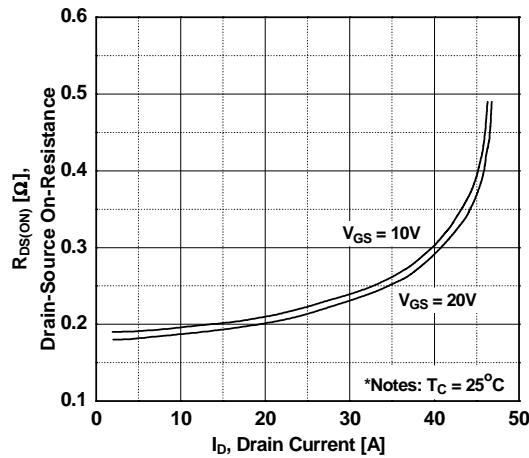


Figure 5. Capacitance Characteristics

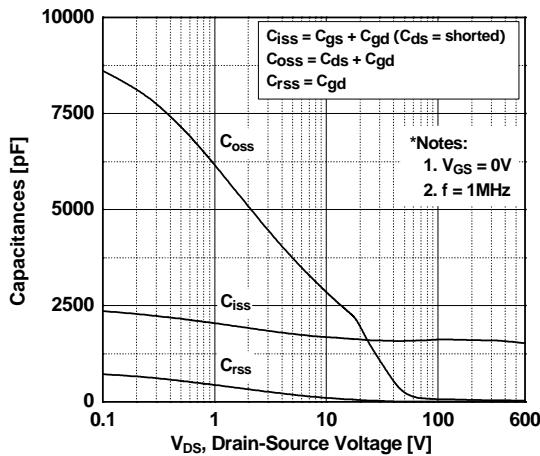


Figure 2. Transfer Characteristics

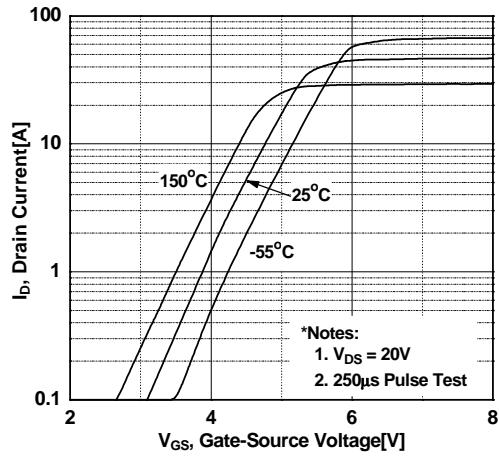


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

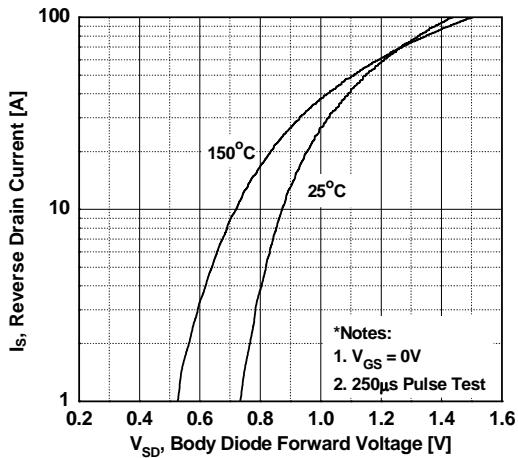
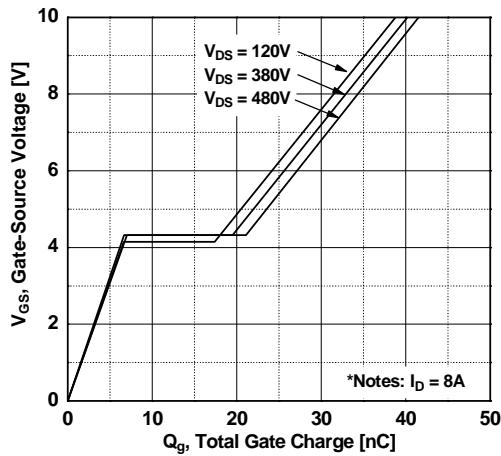


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

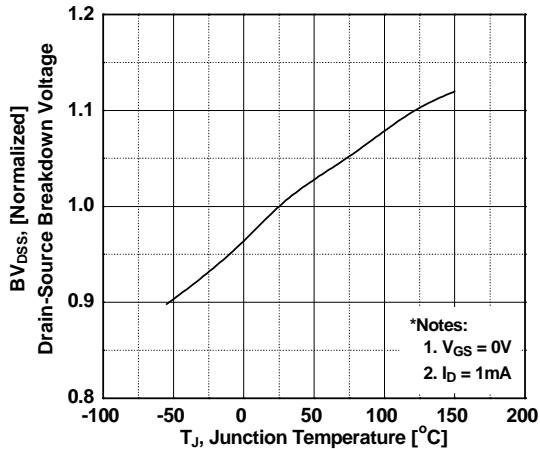


Figure 8. On-Resistance Variation vs. Temperature

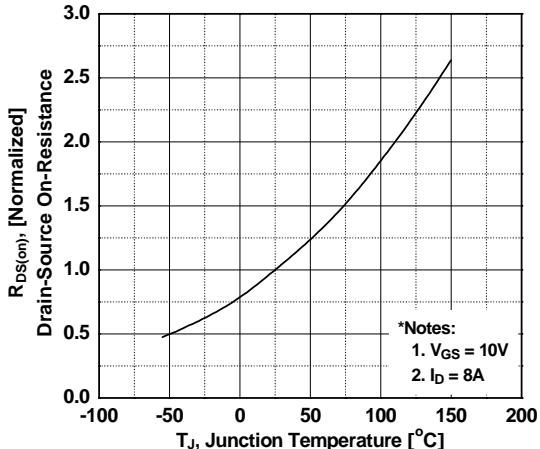


Figure 9. Maximum Safe Operating Area

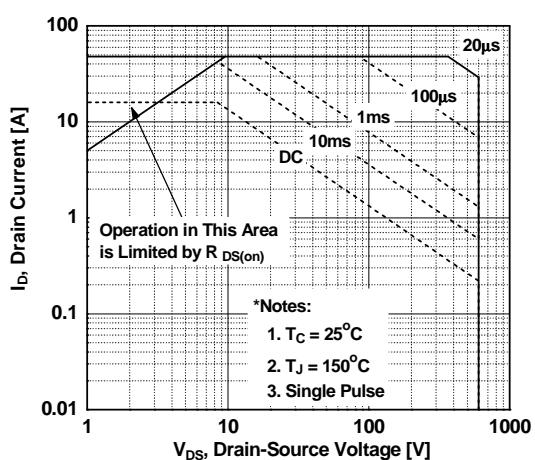


Figure 10. Maximum Drain Current vs. Case Temperature

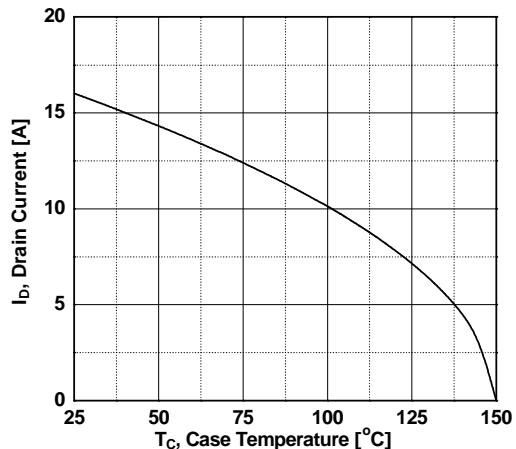
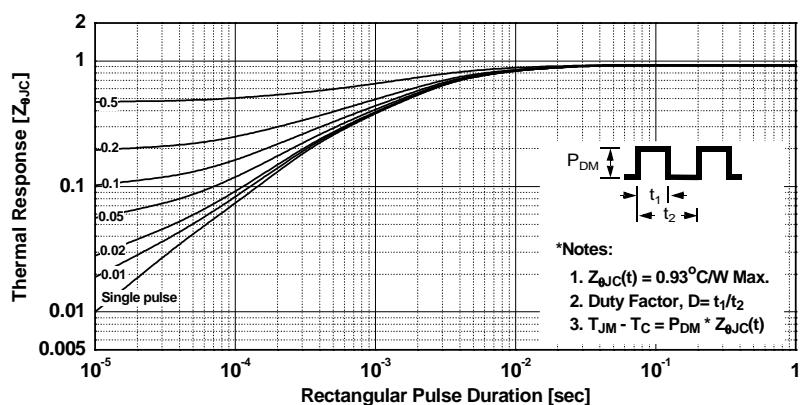
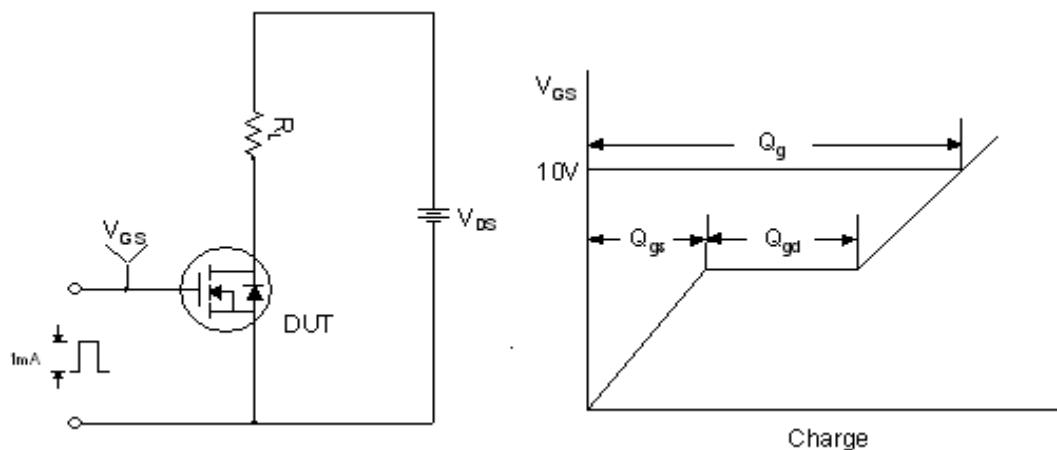


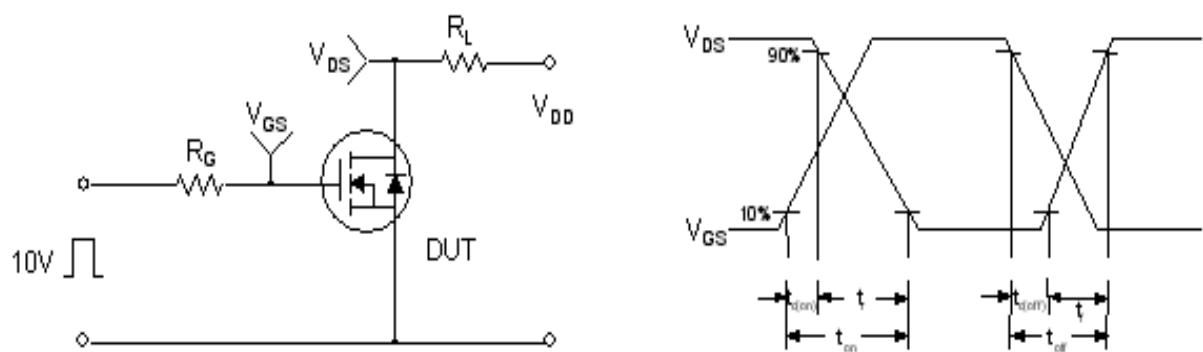
Figure 11. Transient Thermal Response Curve



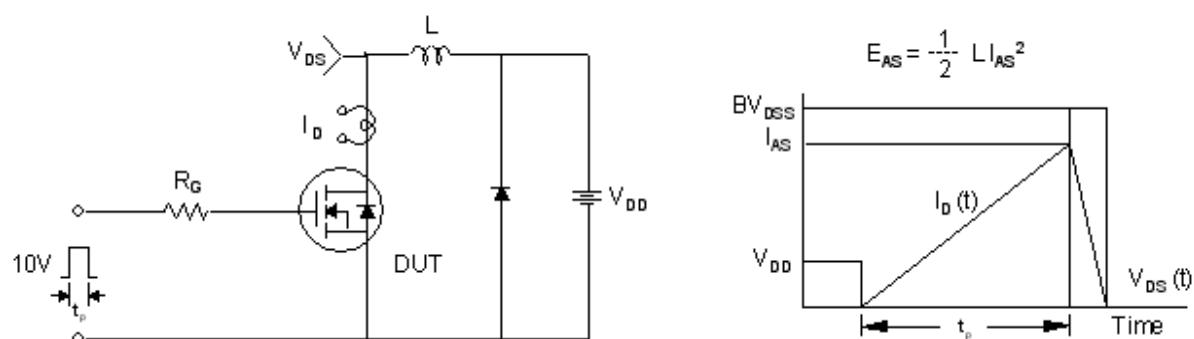
Gate Charge Test Circuit & Waveform



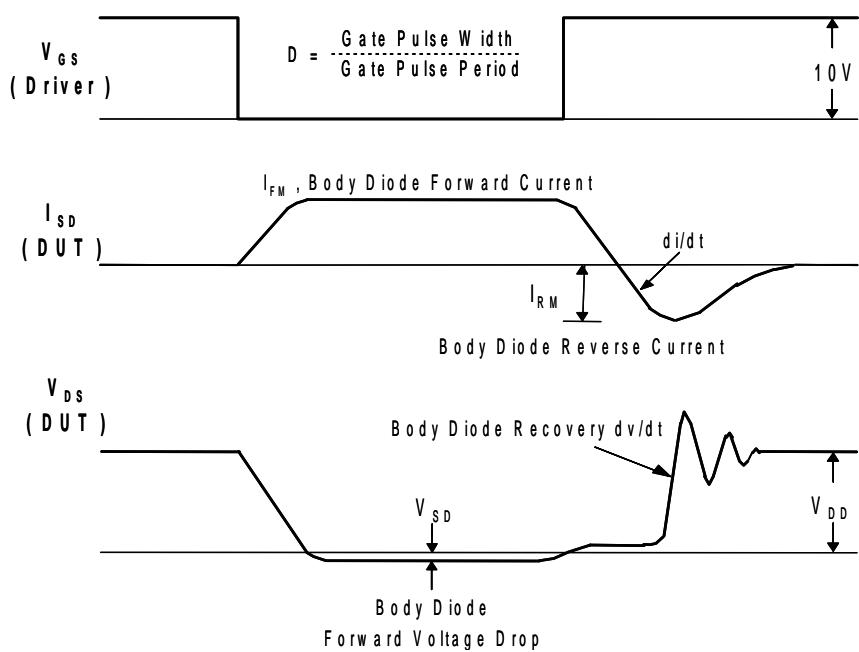
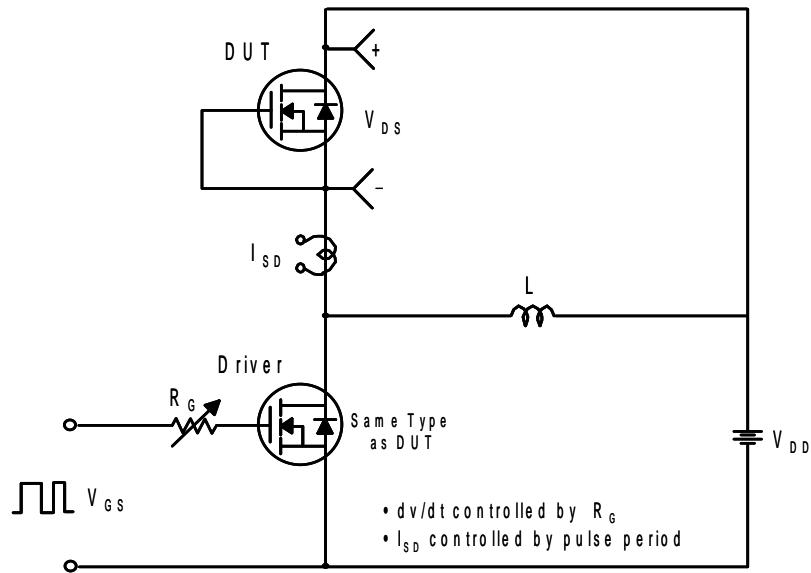
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

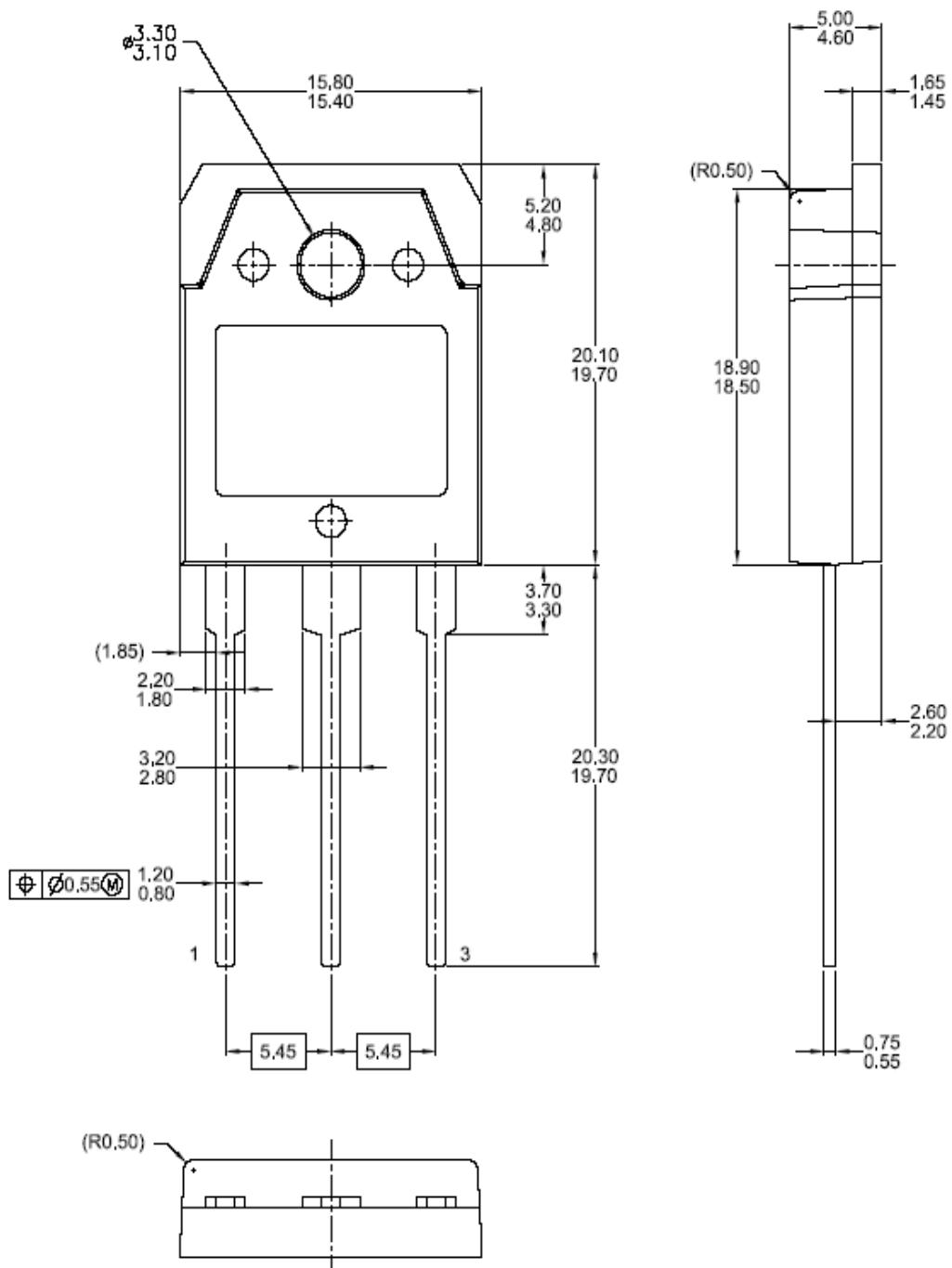


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-3PN



Dimensions in Millimeters



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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